

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

- 1 1. (currently amended) A memory system comprising:
2 a memory controller;
3 an interface device coupled to the memory controller via a first signal path that is
4 permanently terminated at the interface device; and
5 a plurality of memory elements removably coupled to the interface device via respective
6 second signal paths, each of the second signal paths having a lower data transfer
7 capacity than a data transfer capacity of the first signal path.
- 1 2. (original) The memory system of claim 1 wherein the first signal path comprises a
2 plurality of substantially parallel signal lines that extend from a first end at the memory
3 controller to a second end at the interface device.
- 1 3. (original) The memory system of claim 2 wherein the plurality of the signal lines is
2 disposed within a flexible material to form a flex cable.
- 1 4. (original) The memory system of claim 2 wherein the first signal path further comprises a
2 plurality of shielding elements disposed adjacent individual signal lines of the plurality of
3 signal lines to shield the individual signal lines from one another.
- 1 5. (original) The memory system of claim 4 wherein each of the shielding elements is
2 disposed in coaxial alignment with a respective one of the individual signal lines.
- 1 6. (original) The memory system of claim 2 wherein the plurality of signal lines comprise

2 conductive traces disposed on a printed circuit board.

1 7. (original) The memory system of claim 1 wherein the interface device is implemented in a
2 dedicated integrated circuit device.

1 8. (original) The memory system of claim 1 wherein the data transfer capacity of the first
2 signal path is at least as great as a sum of the data transfer capacities of the second signal
3 paths.

1 9. (original) The memory system of claim 1 wherein the first signal path comprises at least
2 one signal line to conduct a first timing signal from the memory controller to the interface
3 device, and wherein the interface device includes circuitry to sample signals on the first
4 signal path in synchronism with the first timing signal.

1 10. (original) The memory system of claim 9 wherein the first timing signal is a clock signal.

1 11. (original) The memory system of claim 9 wherein the first timing signal is a strobe signal.

1 12. (original) The memory system of claim 9 wherein the second signal paths comprise
2 respective signal lines to conduct second timing signals from the interface device to the
3 memory elements, and wherein the first timing signal oscillates at greater frequency than
4 the second timing signals.

1 13. (original) The memory system of claim 12 wherein the oscillating frequency of the first
2 timing signal is an integer multiple of the oscillating frequency of the second timing
3 signals.

1 14. (original) The memory system of claim 1 wherein at least one of the memory elements
2 comprises a memory module having a plurality of discrete memory devices mounted
3 thereon.

1 15. (original) The memory system of claim 1 wherein at least one of the memory elements
2 comprises a plurality of memory modules coupled in parallel to the respective second
3 signal path.

1 16. (original) The memory system of claim 1 wherein at least one of the memory elements
2 comprises a discrete semiconductor memory device.

1 17. (currently amended) A method of operation within a memory system, the method
2 comprising:
3 transmitting multiplexed data from a memory controller to an interface device at a first data
4 rate via a signal path that is permanently terminated at the interface device;
5 demultiplexing the multiplexed data into a plurality of data subsets within the interface
6 device; and
7 transmitting the each of the data subsets from the interface device to a respective one of a
8 plurality of memory elements at a second data rate.

1 18. (original) The method of claim 17 wherein the second data rate is lower than the first data
2 rate.

1 19. (original) The method of claim 17 wherein the first data rate is an integer multiple of the
2 second data rate.

1 20. (original) The method of claim 17 further comprising receiving the multiplexed data
2 within the memory controller.

1 21. (original) The method of claim 17 further comprising receiving a plurality of data values
2 from a host device, and wherein transmitting multiplexed data from the memory controller
3 to the interface device comprises transmitting the plurality of data values to the interface
4 device in respective time intervals.

1 22. (original) The method of claim 17 wherein demultiplexing the multiplexed data into a
2 plurality of data subsets comprises allocating multiplexed data received in the interface
3 device during a first time interval to a first one of the data subsets and allocating
4 multiplexed data received during a second time interval to a second one of the data subsets.

1 23. (currently amended) An interface device for use in a memory system, the interface device
2 comprising:
3 a first input/output (I/O) port to receive multiplexed data from a memory controller at a
4 first signaling rate via a signal path that is permanently terminated at the interface
5 device;
6 demultiplexing circuitry to demultiplex the multiplexed data into a plurality of data subsets;
7 and
8 a plurality of second I/O ports to output the plurality of data subsets to respective memory
9 elements at a second signaling rate.

1 24. (original) The interface device of claim 23 wherein the second signaling rate is slower than
2 the first signaling rate.

1 25. (original) The interface device of claim 24 wherein the first signaling rate is an integer
2 multiple of the second signaling rate.

1 26. (original) The interface device of claim 23 wherein the interface device is implemented in
2 a dedicated integrated circuit device.

1 27. (original) The interface device of claim 23 wherein the demultiplexing circuitry is
2 configured to allocate multiplexed data received during a first time interval to a first one of
3 the data subsets and to allocate multiplexed data received during a second time interval to
4 another one of the data subsets.